

**NMOS VOLTAGE BREAKDOWN CHARACTERISTICS COMPARED WITH
ACCELERATED LIFE TESTS AND FIELD USE DATA**

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Abstract

Statistics on voltage-accelerated failures of 4K NMOS RAM's have been compared with accelerated life test data and with real field use data. It is concluded that it is possible to get long-term reliability information from fast overvoltage step stress tests such as 40 ms and 1.2 s dwell time per step. The correlation between step stress data and life-test failures representing the main population is good. It is possible to use this quick test for lot acceptance and to design a proper voltage screening for the particular batch under test. The need for conventional burn-in testing would thus be reduced.

INTRODUCTION

The usual way to get information on long term reliability is to carry out accelerated life tests at different temperatures and then to extrapolate the result down to the normal use temperature. This process is expensive and time-consuming - typically it includes 1000 h at 125°C and 168 h at 175°C on 250 pcs each, totaling 500 devices. The large number of devices is essential in order to get any failures at all on which to base the failure-rate calculations. It is evident that such a test could be used as a qualification approval exercise but not for a lot acceptance test. Therefore there is still a need for a quick test, reasonably cheap, that gives the same (or possibly more) information about the stability of the device.

This paper describes such a quick test that might be useful for lot acceptance, designing a proper screening method for a particular lot and possibly a reduced qualification approval cost.

THE STEP STRESS TEST

Figure 1 shows the typical test procedure that makes use of the component test equipment only. No additional equipment is needed.

The device is first functionally checked at nominal voltage and then stressed by a static V_{DD} bias for a brief interval. A functional test at nominal voltage is performed again before the next voltage step is applied, now increased by 1 V. The procedure continues until the device fails or the voltage exceeds a certain limit.

The V_{DD} -value at which the device failed is recorded and a new device is tested. This is done on 25 pcs using one stress time, e.g. 40 ms and then repeated on 25 additional devices using another stress time, e.g. 1.2 s.

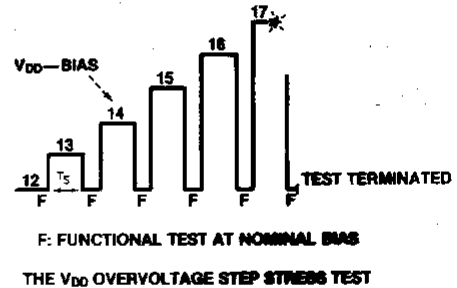


Figure 1

EVALUATION OF DATA

The 50% breakdown voltage levels for the two stress durations $V_{50}(t_1)$ and $V_{50}(t_2)$ respectively, are determined from the breakdown voltage statistics.

A coefficient β for the voltage dependence of the time to 50% failures is defined as follows:

$$\beta = \ln(t_2/t_1) / (V_{50}(t_1) - V_{50}(t_2)) \quad [V^{-1}] \quad \dots(1)$$

See also ref. 1 where a similar notation has been used.

If the device is going to be used at a voltage V , then the time to 50% failures would be $t_{50}(V)$.

$$t_{50}(V) = \exp(\beta(V_{50}(t_2) - V)) \cdot t_2 \quad \dots(2)$$

The dispersion σ is determined by the Cdf-levels Q_1 and Q_2 measured at a fixed voltage at the end of the two stress dwell times t_1 and t_2 .

$$\sigma = \log(t_2/t_1) / (X_1 - X_2) \quad [\text{decades}] \quad \dots(3)$$

Here $Q(X_1) = Q_1$ and $Q(X_2) = Q_2$; see also Appendix 1 for a rational expression for calculation of X .

Once the median life t_m and the dispersion are known, the failure-rate is easily determined by common log-normal formulas.

The temperature dependence is first approximated by a simple Arrhenius equation. Equation (2) then becomes:

$$t_{50}(V, T) = \exp(11605 \cdot E_A \cdot (1/(273+T) - 1/(273+T_0))) \cdot \exp(\beta(V_{50}(t_2) - V)) \cdot t_2 = t_2 \cdot f_1(T, T_0) \cdot f_2(V) \quad \dots(4)$$

Here E_A = Activation energy (eV)

T_0 = Test temperature at which $V_{50}(t_2)$ was determined (°C)

The influence of burn-in or a short voltage screening is calculated simply by moving forward in the failure-rate curve by the same amount of field use time that the screening simulates. A voltage-stress test V_s at temperature T_0 for a time t_s will thus be equivalent to t at voltage V and at the field use temperature T where

$$t = t_s \cdot f_1(T, T_0) \cdot \exp(\beta(V_s - V)) \quad \dots(5)$$

The real field use time then starts not from zero but from t according to equation (5).

The breakdown voltage values are plotted on a normal distribution diagram. See Figure 2. If data from the two groups with stress dwell times 0.04 s and 1.2 s per step respectively, overlap, then the devices are good, otherwise not so good.

Figure 2 gives an example of evaluation. By reading the median voltage values V_1 and V_2 and the Cdf-levels Q_1 and Q_2 at a fixed voltage, then the β , t_m and σ are calculated with the help of equations (1), (2) and (3).

The values so estimated for β and σ can be used to calculate the total Cdf-function during all the step stress intervals. The Cdf-level is first calculated for stress Level No. 1 during the first dwell time. During the next dwell time the total Cdf-level continues to increase, but now according to another Cdf-function that is determined by the second stress level. Remaining steps are calculated similarly. Appendix 1 gives a more detailed description of the method and the formulas that are used.

DEVICES USED FOR STEP STRESS TESTING

As a part of a qualification approval exercise on 4K dynamic RAM's, around 3000 devices representing different manufacturers and types were life tested for 168 h at 175°C or 1000 h at 125°C. This was done at the beginning of 1978, (Ref. 2). Some of the tested types were still left in the QA laboratory because the solderability might have been degraded during the burn-in or because of other reasons. One way to make use of the devices was to carry out a voltage step stress testing on these devices to see if there was any correlation between life test results

and the voltage overstress data. In order to get an estimate of the Cdf¹-values of fresh (not life-tested) devices during the step stress test, a correction had to be made. If S% previously had been screened away, the corrected Cdf¹-values were calculated using equation (6)

$$Cdf^1 = s + Cdf(100-s)/100 \quad \dots(6)$$

This small correction has been used on all data except for the data given in Figure 6, where we are interested to see the freak level that still remains after the life test screening.

Around 250 devices were used in each life test reported in this paper. Typically 245 devices survived and from these survivors at least 25 + 25 devices were taken for the step stress testing.

RESULTS

Figure 2 shows the step stress test result from type No 1. As this type had been life tested at two temperatures, it was possible to calculate the Cdf-level at 25°C both from the life tests and from the voltage step stress test. The result of the calculations is given in Figure 3. It is obvious that the two tests gave roughly the same prediction. According to the failure analysis carried out by the manufacturer, most life test failures were due to a leakage current through an isolation oxide (between Metal and Polysilicon) that became degraded with time.

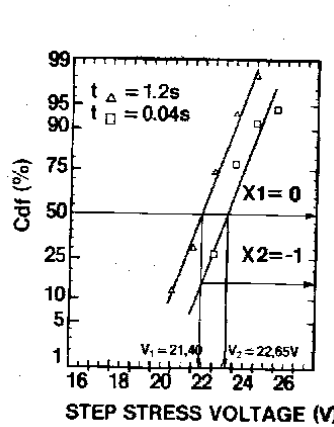


Figure 2

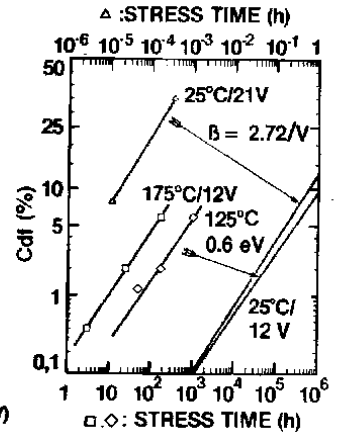


Figure 3

Figure 4 shows the breakdown characteristic of type No. 2. The result indicates a very stable batch. This was verified by the life test at 175°C that gave no failures during a test period of 260 h on 250 devices. See Figure 5.

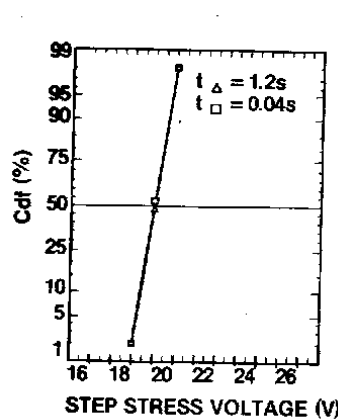


Figure 4

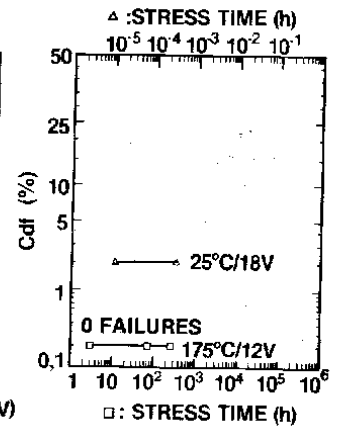


Figure 5

Type No. 3 was life-tested at 175°C and 125°C (See Figure 7). 150 devices were stressed by a V_{DD} -bias of 21 V instead of the nominal 12 V. Then the parts were inspected by a MARCH-function test after 1-3-7-15-.....-1023 ms. The corresponding Cdf-function is shown in Figure 7 and it is clear that the slope is not the same as the one obtained from the life tests.

As the Cdf-level increased rather linearly with time during the life tests, one is led to suspect that the batch had been screened by the manufacturer. The solid lines through the life-test data points are calculated using the following parameters:

Median Life $t_m = 8 \cdot 10^{14}$ h; $\sigma = 10$ decades; $E_A = 0.8$ eV.

The calculation assumes that the manufacturer has performed a voltage screening equivalent to $3 \cdot 10^5$ h of field use at 25°C .

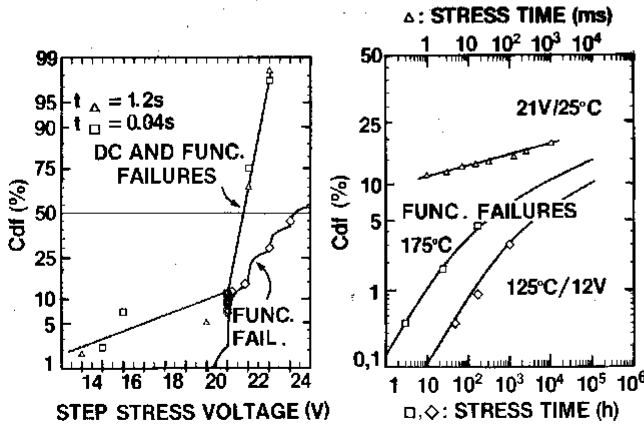


Figure 6

Figure 7

Figure 6 shows the functional failures (\diamond) and DC + functional failures (Δ , \square) during voltage step stressing. The curved solid line is calculated using the same life distribution as before. All previous screenings (including life-test) were set equivalent to 1 s at 20 V with $\beta = 4.7$ /V. DC-failures were caused by a field MOS-transistor that turned on and increased the power consumption permanently. Functional failures were related to pn-junction leakage degradation and breakdown.

The curve-fitting exercise shows that the life-tests and voltage overstress tests are in agreement. The manufacturer has probably been using an overvoltage screening in the order of 1 s/16.5 V, which in this case has eliminated 20 % of the population. The manufacturer has admitted that voltage stressing is a part of their production testing.

The data in Figure 6 have not been corrected according to equation (6), but are the measured Cdf-levels on devices that already have been life-tested for 168 h at 175°C . The 21 V-data of figure 7 has, however, been corrected in order to estimate the future slope of the life-test data.

Type No. 4 was a rather stable one according to the breakdown data shown in Figure 8. There is, however, always a possibility that a small freak subpopulation exists, since the sample consists of only 50 items. The life-test at 175° shows that a few % failures should be expected, at least at this temperature. See Figure 9. Type No. 4 was also used to characterize the temperature dependence of the breakdown voltage. As can be seen from Figure 10, a few % of the population have a reduced breakdown voltage level at both 150°C and 175°C . Thus some agreement between the life-test and the step stress test has been established.

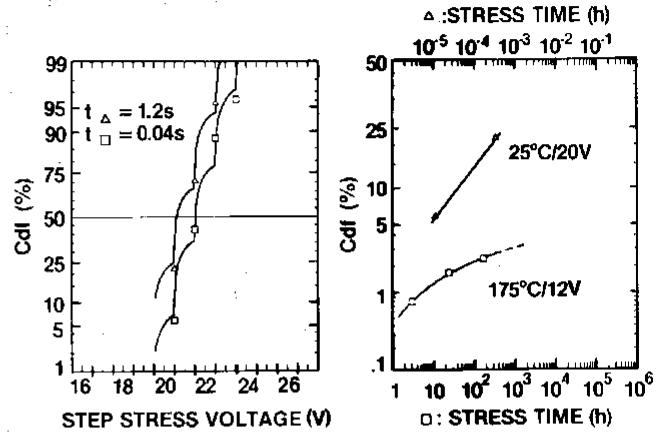


Figure 8

Figure 9

To summarize: The main failure/voltage distribution will normally be determined by a field oxide MOS-transistor that turns on around 20 V. An impure and unstable field oxide will be detected by the step stress test. Thin oxide breakdown voltages should exceed the parasitic MOS-transistor turn-on voltage, but "freak", low breakdown values can be found and possibly screened away.

THE TEMPERATURE DEPENDENCE OF BREAKDOWN FAILURES

Time-dependent breakdown mechanisms are often modelled using one temperature- and one voltage-dependent factor as is done in equation (4). The temperature dependence has been connected with activation energies ranging from 0.3 to 2.1 eV (Ref. 1.4). Life test studies on memory devices (Ref. 3) also indicate that the effective activation energy could change with temperature.

Samples of type No. 4 were used for voltage step stress testing at 25, 60, 100, 150 and 175°C . Figure 10 shows the failure voltage distributions. The main failures were caused by a field MOS transistor that turned on for V_{DD} -levels around 20V. The increase in failure threshold voltage with temperature could e.g. be due to electron injection and trapping within the field oxide. No real failure analysis was carried out, however.

At 175°C the first failures were induced at a voltage less than 20V. By comparing figures 9 and 10 one might say that 1.2 s/18V is equivalent to 3500 h/12 V. This gives $\beta = 2.7$ /V or an acceleration factor of 10^7 /MV/cm for $t_{ox} = 600\text{Å}$, assuming that these failures were due to gate oxide degradation.

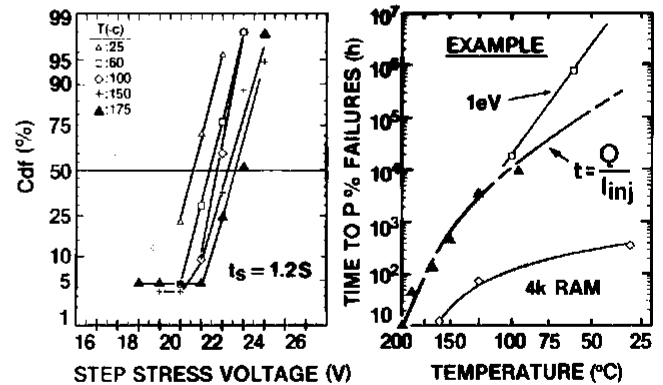


Figure 10

Figure 11

It has also been reported (Ref. 5, 6) that the breakdown voltage of thin oxide is increasing with temperature. Such an increase in voltage margin at high temperatures would imply a reduction of the effective activation energy of the time to failure. If hot electron injection may change the electric field over a weak oxide then the time to failure would have a temperature dependence similar to that of $1/I_{inj}$. Measured values of gate current vs temperature are given in figure 6 of Ref. 9. Figure 11 shows this inverted gate current times a constant together with life test data of 4K RAM's according to Ref 3. Both set of data indicates that the effective activation energy will increase with temperature.

DEPENDENCE ON CHIP AREA

Appendix 2 gives a statistical analysis of the influence of chip area on Cdf-values. It is shown that the failure rate is expected to be proportional to the chip area.

FIELD FAILURE STATISTICS

Figure 12 gives the test result at 175^oV and the following field use failure statistics of a 4K MOS-RAM. Figure 13 shows test and field failure data for 16K MOS-RAM's. The activation energies are 1 and 0.8 eV respectively.

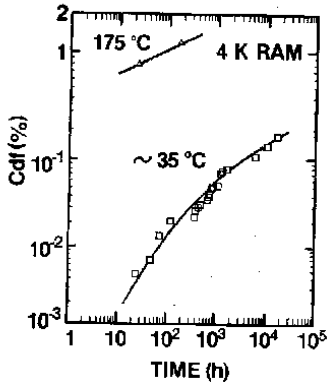


Figure 12

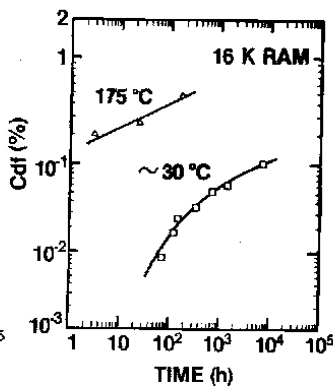


Figure 13

△: 500 4k ; 1500 16k
 □: 43000 4k ; 11500 16k

VOLTAGE-STRESS SCREENING

A screening that occupies a component tester should not take more than, say, 10 s to carry out, let us call the time t_s . If this screening is to simulate the time t_{fs} e.g. the first few weeks in field, then the stress over-voltage ΔV is

$$\Delta V = \ln(t_{fs}/t_s)/\beta \quad \dots(7)$$

In order to get practical experience from voltage screening, a batch consisting of 22 000 4K dynamic RAM's was used. First, a step stress test was carried out on 50 random samples. The result of the step stress test indicated that the batch was stable and that few failures should be expected in a voltage screening. A screening program was designed that stressed 11 000 devices by a V_{DD} pulse of 15.6 V for 2 s and then checked the parts by a MARCH-test for function at nominal voltage. Parts were mounted on memory boards which were tested. Boards with both screened and non-screened parts were MARCH-tested for 24 h at 55^oC. Memory modules were then used for 1000 h at 25^oC. Table 1 gives the results in detail. A few conclusions can be drawn immediately:

- As a significantly larger amount of AC-failures was noted in the PC-board test for screened compared with the non-screened parts, the screening should be concluded with a complete test program and not only with a MARCH-function test
- The total amount of functional failures was small and in agreement with the expectation from the step stress test
- The field failure rate of the screened parts seems to be lower than the failure rate of the non-screened parts.

With all reservations made due to the very limited number of failures, one might take a closer look at the failure time data in table 1. Figure 14 shows the Cdf-Level of field failures from voltage screened and non-screened parts. The Cdf-function for the non-screened parts passes 0.055% after 30 h of field use. As 0.055% of the devices were eliminated during the voltage screening, a Cdf-function was calculated for the case where parts had been screened for 30 h at field use conditions. This calculated line is shown in Figure 14. The Cdf-data points from the screened parts are very close to the calculated line and it is fair to say that in this case 2s/15.6 V is equivalent to 30 h/12 V. According to equation (7) this corresponds to $\beta = 3.0/V$. For a thin oxide of 600Å this represents an acceleration factor of $10^{7.8}/MV/cm$.

The corresponding failure-rate curves are calculated and presented in Figure 15.

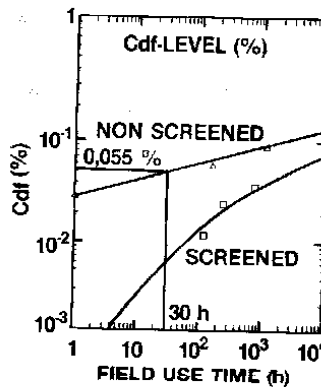


Figure 14

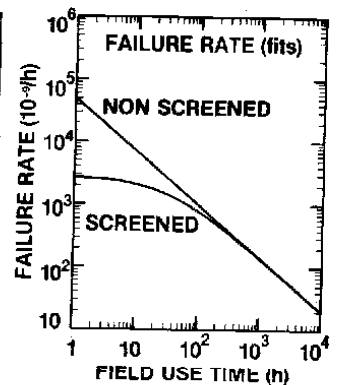


Figure 15

Activity	No. Tested	% failed	% failed
Incoming	22 000	1.5	1.5
Screening $V_{DD} = 15.6 V/2 s$	11 000	---	0.055
Board Testing	Non-scr. 9 800 + Scr. 9 800	Non-screened Func. AC 0.051 0.163	Screened Func. AC 0.031 0.316
Module testing 24 h 55°C	9 300 + 9 300	AC 0.022	AC 0.022
Field use 1000 h 25°C	3456 + 8064	Time 7 h 0.029 160 h 0.058 1150 h 0.087	Time 120 h 0.012 240 h 0.025 760 h 0.037

Table 1

Summary of all failures from incoming inspection to field use of voltage screened and non screened 4K MOS dynamic RAM's.

CONCLUSIONS

Voltage step stress testing of dynamic NMOS-LSI devices may be a rapid way of getting reliability information. The method is primarily suited for dynamic parts with low static power dissipation. Static parts will be overheated.

A sample size of 25-50 pcs will permit a characterization of the main population while a still larger number of devices is needed to get quantitative data on "freak" populations. The latter applies to thin oxide breakdown.

The step stress test could be used as a complement to a standard life test to determine whether the test failures belong to a sub-population or are representative of the main population. It may also provide information on the screening level applied by the manufacturer.

Step stress test data may also be evaluated in order to get a screening test optimally designed for a particular batch of devices.

ACKNOWLEDGEMENTS

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Appendix 1

EVALUATION AND SIMULATION OF VOLTAGE STEP STRESS TESTS

Ref. (7) gives a good description of a general method for step stress analysis. In the present case, this method has been applied using a log-normal distribution of the time to failure. The first set of values of β , σ and median life has been estimated as outlined in the paper, and then, if necessary, minor modifications have been introduced by "cut and try" to get a better fit to the data.

Using the same type of notation as in Ref. (7) the following equations will apply. The Cdf of time to failure under a particular step stress pattern is called $F_0(t)$. During the first step $0 < t < t_1$ the Cdf will of course follow the steady state stress function $F_1(t)$ i.e.

$$F_0(t) = F_1(t) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_1} \exp(-x^2/2) dx \quad \dots(A1)$$

where

$$x_1 = \log_{10} (t/t_m(V_1))/\sigma \quad \dots(A2)$$

$$\text{In general } F_1(t, Y_1) = (F_1(t) - F_1(Y_1)) / (1 - F_1(Y_1)) \dots(A3)$$

Here $t_m(V_1)$ = median life time at voltage V_1 in step i and Y_1 represents the equivalent amount of pre-screening time at stress voltage V_1 that has been applied to the device before the step stress test. The dispersion throughout this paper is expressed in decades.

During the next step the aging process will go faster and follow another steady stress function $F_2(t)$ starting from the equivalent time S_1 , found by solving equation (A4).

$$F_2(S_1) = F_1(t_s) \quad \dots(A4)$$

Equation (A4) will in this case become

$$\frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_2} \exp(-x^2/2) dx = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{x_1} \exp(-x^2/2) dx$$

$$\text{or simply } x_2 = x_1 \quad \dots(A5)$$

If one knows the Cdf-value p that represents the amount of failures accumulated during the first step, the corresponding $x_p = x_1$ can be calculated using rational expressions like the one given in Ref. (8) para. 26.2.22

$$x_p = u - (a_0 + a_1 u) / (1 + b_1 u + b_2 u^2); u = \sqrt{(\ln p^{-2})}$$

which is valid for $0 < p < 0.5$

$$a_0 = 2.30753; a_1 = 0.27061; b_1 = 0.99229; b_2 = 0.04481$$

This equation (A5) with the help of equation (A2) transforms to equation (A6)

$$S_1 - Y_2 = t_m(V_2) \cdot \exp(x_p \cdot \sigma \cdot \ln 10) \quad \dots(A6)$$

The median life at V_2 is as earlier

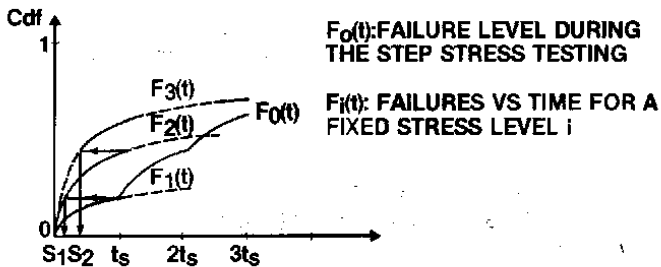
$$t_m(V_2) = t_m(V_0) \cdot \exp(\beta(V_0 - V_2)) \quad \dots(A7)$$

where $t_m(V_0)$ has been estimated from the step stress results.

$$\text{Similarly } Y_2 = Y_1 \cdot \exp(\beta(V_1 - V_2)) \quad \dots(A8)$$

The total Cdf $F_0(t)$ during the second step will now grow according to $F_2(S_1 + t)$; $t \geq 0$, but actually starting at the time $t = t_s$ instead of S_1 as visualized beneath.

The remaining steps are calculated similarly.



CALCULATION OF FAILURE LEVEL $F_0(t)$

Appendix 2

CHIP AREA DEPENDENCE

It is reasonable to assume that voltage induced failures are located at specific points on the chip where the internal structure just happens to have a weakness. In real field use the supply voltage is nearly constant and the number of weak spots that are sensitive for that voltage must be of importance for the reliability of the device. Let us make the following definitions:

The time to failure for a certain weak spot number i is called X_i . This time X_i has the distribution $F_i(x) = P(X_i < x)$. On a single chip we will have N weak spots with a certain probability; $p_v = P(N = v)$; $v = 0, 1, 2, \dots$. The time to failure for a device having exactly N weak spots will be Z_N with its distribution $G_N(z)$

$$\begin{aligned} G_N(z) &= P(Z_N \leq z) = 1 - P(Z_N > z) = \\ &= 1 - P(X_1 > z, X_2 > z, \dots, X_N > z) = \\ &= 1 - P(X_1 > z) \cdot P(X_2 > z) \cdot \dots \cdot P(X_N > z) = \\ &= 1 - (1 - F_1(z)) \cdot (1 - F_2(z)) \cdot \dots \cdot (1 - F_N(z)) \end{aligned}$$

assuming X_1, X_2, \dots are statistically independent variables. As all X_i have the same distribution, all $F_i(z)$ will be equal, and hence

$$G_N(z) = 1 - (1 - F(z))^N \quad \dots(B1)$$

Normally one does not have information on the number of weak spots N that exist in a specific device. If $p_v = P(N = v)$ then the N -independent distribution of time to failure will be:

$$G(z) = \sum_{v=0}^{\infty} p_v \cdot G_v(z) = \sum_{v=0}^{\infty} p_v [1 - (1 - F(z))^v] \quad \dots(B2)$$

Assume that N has a Poisson distribution with a mean value αA ; α = expected number of weak spots per unit area and A = chip area of interest.

$$\text{Then } p_v = \frac{(\alpha A)^v}{v!} e^{-\alpha A} \quad (v = 0, 1, 2, \dots)$$

$$\begin{aligned} \text{and } G(z) &= \sum_{v=0}^{\infty} \frac{(\alpha A)^v}{v!} e^{-\alpha A} [1 - (1 - F(z))^v] = \\ &= 1 - \sum_{v=0}^{\infty} \frac{(\alpha A)^v}{v!} e^{-\alpha A} (1 - F(z))^v = \\ &= 1 - e^{-\alpha A} \sum_{v=0}^{\infty} \frac{[\alpha A \cdot (1 - F(z))]^v}{v!} = \\ &= 1 - e^{-\alpha A} e^{\alpha A (1 - F(z))} = \\ &= 1 - e^{-\alpha A \cdot F(z)} \quad \dots(B3) \end{aligned}$$

Note that $\lim_{z \rightarrow +\infty} G(z) = 1 - e^{-\alpha A} < 1$. This is due to the fact that if $N=0$, i.e. there is no weakness, the time to failure will be infinite. This happens with the probability $P(N=0) = e^{-\alpha A}$, hence the probability that the time to failure will be finite is $1 - e^{-\alpha A}$, which agrees with the limiting value of $G(z)$ as z approaches infinity.

If a test structure of area A has been tested and the life distribution $G(z)$ is characterized, then the time z to failure for a single weak spot will have a distribution $F(z)$.

$$F(z) = -\frac{1}{\alpha A} \ln(1 - G(z)) \quad \dots(B4)$$

A device using the same technology (same α) but having another area A^1 will then get a life distribution $G^1(z)$.

$$G^1(z) = 1 - \exp\left(-\frac{A^1}{A} \ln(1 - G(z))\right) = 1 - (1 - G(z))^{A^1/A} \quad \dots(B5)$$

With $A^1/A = a$ the failure rate will be

$$\frac{dG^1(z)}{dz} = a (1 - G(z))^{a-1} \cdot \frac{dG(z)}{dz} \approx a \cdot \frac{dG(z)}{dz} \quad \dots(B6)$$