ACCELERATION FACTORS FOR TEMPERATURE-HUMIDITY TESTING OF Al-METALLIZED SEMICONDUCTORS

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ABSTRACT

Different temperature-humidity tests have been conducted on plastic encapsulated and decapsulated CMOS microcircuits to determine how the test parameters effect the device life time. Together with published data from other temperature-humidity tests, 51 acceleration factors relative to the 85/85 test have been collected. The data is compared with four proposed models for THB-tests.

One of the models has been used in order to estimate the acceleration factor for hermetic encapsulated semiconductors with trapped moisture. It was found that 2000 ppm of trapped moisture should be the maximum allowed level for microcircuits, for use in Telecommunications equipment.

It is concluded that plastic encapsulated semiconductors having<5% failures after 500h in an 85/85 test would be accepted for telecommunication use in certain environments.

INTRODUCTION

The use of plastic encapsulated microcircuits in telecommunication equipments has been restricted, mainly because of the wear-out mechanisms due to moisture that effects the reliability of semiconductors. Although a lot of telecommunication equipment is used in well controlled environments, the difficulty in translating results from accelerated temperature-humidity tests to the normal environments has prevented their use in applications where they probably could be utilized.

In order to get a better understanding of the correlation between different combinations of temperature-humidity tests, a study was undertaken on CMOS devices where the median lifes at certain T/RH-tests were compared with the median life at 85/85. In addition to that data a literature study was carried out and a total 51 different acceleration factors were obtained. The material was analyzed on order to see if any of the existing published models for T/RH-acceleration factors would fit the data. Two out of four tested models seem to correlate well with the data. One is very simple to use for approximate estimates, and the other gives a more accurate result.

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The problem of corrosion due to trapped moisture inside hermetic devices is an important area to be investigated. At low temperatures the relative humidity will increase and corrosion could occur. Assuming, as a worst case, that cooling below the freezing point of water would not initiate a drastic decrease in surface conductivity, then the second model has been used to estimate the median life for different levels of trapped moisture.

Finally, field statistics on failures due to corrosion of non-hermetic MOS-memories is compared with the expected life according to the acceleration factors collected.

SURFACE CONDUCTIVITY AND CORROSION

Surface conductivity is an important factor that determines the rate of corrosion. Several investigations have been reported on the influence of temperature and relative humidity on the surface conductivity of SiO_2-devices. Figures 1 and 2 are examples taken from Reference 1 for plastic encapsulated SiO_2. The data points have been plotted in log-normal distribution diagrams in an attempt to get stright lines as the curves normally tend to be S-shaped when RH is plotted on a linear scale.

From figures 1 and 2 it seems reasonable to assume that the acceleration factors between different T/RH-combinations should have an Arrhenius temperature dependence and a non linear RH-dependence.

$$A(T/RH) = A_1(T) \times A_2(RH) \qquad \ldots(1)$$

$$A_1(T) = \exp\,(11605 \times E_A \times (1/(273+T) - 1/(273+85))) \qquad \ldots(2)$$

The only non-linear function proposed in the literature is the use of $(RH)^2$ between 25-100% RH (Ref 2). This model gives:

$$\log_{10} A_2(RH) = k(85^2 - RH^2), \qquad \ldots(3)$$

where k is the slope in a diagram with $(RH)^2$ plotted on a linear scale.

Koelmans (Ref 3) has pointed out that droplets could form on a chip surface under bias in a humid environment and thereby accelerate the corrosion process in certain spots. Most of the data in the present paper indicates, however, that the acceleration factors for THB-tests are similar to those that can be calculated from surface conductivity measurements.

CMOS THB-STUDY

The Temperature-Humidity-Bias (THB)-test on CMOS devices was divided into two parts. Part one consisted of 1000 CMOS microcircuits type 4001 in plastic encapsulation. These devices were split up into four groups that were put into different THB-tests according to Figure 3. Part two consisted of 96 decapsulated CERDIP encapsulated CMOS microcircuits, also type 4001. These devices were split into 6 groups and tested with different THB-conditions according to Figure 4.

The plastic encapsulated devices were electrically tested by a computer controlled tester on several occasions during the THB-test. All deviations from the specification were classified as failures. The delidded devices were optically inspected for signs of corrosion and the cumulative number of corroded devices was noted during the test. Tables 1 and 2 give a summary of Figures 3 and 4 in respect of acceleration factors relative to the 85/85 test. As the median life for decapsulated devices at 85/85 is short it is possible to get acceleration factors for low temperatures at low levels of humidity.

Table 1

T(^{o}C)	RH(%)	$t_{5\%}$(h)	A
85	85	450	1
65	95	600	1.3
65	85	3 000	6.7
45	95	3 000	6.7

Acceleration factors for 5% failures according to tests on plastic encapsulated CMOS-devices (Figure 3).

Table 2

T(^{o}C)	RH(%)	$t_{50\%}$(h)	A
85	85	15	1
85	55	150	10
85	20	1 500	100
20	85	7 500	500
20	58	30 000	2 000
20	26	80 000	5 300

Acceleration factors according to tests on decapsulated CMOS devices (Figure 4).

MODELS FOR ACCELERATION FACTORS

A literature search of mainly Reliability Physics since 1970 and other reports was conducted to find other examples of acceleration factors relative to the 85/85 test. In some cases tests at 85/85 had not been carried out so the median life at 85/85 had to be estimated from the data presented. Normally there was a test very close to 85/85 so the error is thought to be insignificant.

Figure 5 shows the data points collected. The solid lines are computed according to eqn (1) with $E_A = 0.8$ eV and the slope $k = \log 60/(85^2-25^2)$. It is apparent that the model fits the data well. Figure 6 shows the same data points as a function of the reciprocal of the partial pressure of water, $10^4/Vp$ (Ref 4). This model does not seem to be useful. Figure 7 shows the data points plotted as a function of the partial pressure of water, which has also been proposed (Ref 5). Again, this model does not seem to be particular useful. Figure 8 shows the data points plotted in an Arrhenius diagram. Reich-Hakim have proposed (Ref 6) that the numerical sum of T (°K) and RH (%) should be used instead of T (°K) in an Arrhenius model. As can be seen this gives a very good model. By regression analysis the slope has been determined to $E_A = 1.19$ eV and therefore a simplified expression for the acceleration factor relative to 85/85 would be:

$$A(T/RH) = \exp(11605 \times 1.19 = (1/(273 + T(^{\circ}C) + RH(\%)) - 1/(273+85+85))) =$$
$$= 2.9 \times 10^{-14} \exp(13810/(T(^{\circ}K) + RH(\%))) \qquad \ldots(4)$$

Finally Figure 9 compares the $(RH)^2$-model and the (T+RH)-model. It is evident that they support each other and both could be used with about the same result.

THE USE OF PLASTIC ENCAPSULATED SEMICONDUCTORS IN TELECOMMUNICATION EQUIPMENTS

The reliability requirements of components used in telecommunication equipments can be summarized as follows:

A: During service life (up to 40 years) no failures due to wear-out of the main population are acceptable.

B: The failure-rate due to weak parts (freaks) shall not exceed certain mean values and the total amount of failures in service shall be less than 0.1 - 2% depending on the device type.

Plastic encapsulated semiconductors may in general have a larger amount of freaks than hermetic parts, but in most cases it should be possible to find manufacturers of plastic encapsulated devices that can meet requirement B.

Plastic encapsulated semiconductors will be affected by moisture and failures for example open circuits on Al-metallization, gold ball bond lifts and increased leakage currents etc., may occur. All such failures are wear-out failures and it is important that they will not occur within 40 years in the specified room ambient.

An example of a specified room ambient is 30°C/80% RH. According to Figure 8 the acceleration factor is 100. This implies that the testing time at 85/85 should be 40 years/100 = 3500h with no failures other than freaks - say maximum of 5%. Normally, this is a too stringent requirement for commercially available plastic devices and hence we could not recommend plastic encapsulated semiconductors for this application. If, however, the device is heated by surrounding components the relative humidity around the chip will be reduced. A 10°C temperature increase from 30°C will reduce the relative humidity from 80% to 43% (See e.g. Ref 7). According to Figure 9 the acceleration factor for 40°C/43% RH is 1000 and therefore the testing time at 85/85 should be 40 years/1000 = 350h. This is a quite reasonable requirement and thus it is concluded that plastic encapsulated semiconductors could be used in telecommunication applications provided the temperature of the biased chip is 10°C above the room ambient, due to power dissipation from surrounding components.

In case the device itself develops power the relative humidity around the chip will be reduced both in the application and in the 85/85-test. Table 3 shows the effective RH around the chip as a function of temperature increase due to power dissipation. The table also gives the acceleration factors relative to 85/85-tests according to eqn (4) assuming no power dissipation.

For a temperature increase of 10°C the 85/85-test actually becomes a 95/58-test and the acceleration factor between that test and the use at 40/43 is 1000/3.48 = 287. The testing time of 95/58 should then be 40 years/287 = 1200 h. Similar calculations could be carried out for other ambients.

△T(%)	T/RH	A
0	85/85	1
1	86/82	1.15
2	87/79	1.33
3	88/76	1.54
4	89/73	1.78
5	90/70	2.06
6	91/67	2.39
7	92/65	2.57
8	93/63	2.77
9	94/60	3.22
10	95/58	3.48

Table 3

Effective T/RH around chip in an 85/85-test as a function of chip over temperature due to power dissipation.

HERMETIC DEVICES WITH TRAPPED MOISTURE

Several papers have reported on failures of hermetic encapsulated devices due to corrosion (See e.g. Ref 8). The corrosion is caused by moisture trapped in the cavity of the device. In the following we will use the model for acceleration factors derived earlier (egns (1) - (3)) to estimate the temperature dependence of the life of hermetic devices containing certain levels of moisture.

The relative humidity RH is defined by eqn (5).

$$RH\ (\%) = \frac{\text{water vapor present at } T^{o}C}{\text{saturated water vapor at } T^{o}C} \times 100 \qquad \ldots(5)$$

If the athmospheric pressure inside the device cavity is P mmHg (normally around 0.5 Atm for a hermetic CERDIP) and the moisture content given in ppm_v, then the water vapor pressure would be:

$$P_w\ (\text{mmHg}) = P \times ppm_v \times 10^{-6} \qquad \ldots(6)$$

An approximation of saturated water vapor pressure P_{ws} between -25^oC and $+25^oC$ is given by eqn (7). This equation is a linear approximation of the partial water vapor pressure on an Arrhenius diagram and is accurate to $\pm 1^oC$. (See e.g. Ref 9 regarding water vapor pressure).

$$P_{ws}\ (\text{mmHg}) = 10^{10} \times \exp(-5899/(273+T)) \qquad \ldots(7)$$

The Dew Point (DP) is then:

$$DP(^oC) = 5899/(\ln 10^{10} - \ln(ppm_v \times P \times 10^{-6})) - 273 \qquad \ldots(8)$$

Equations (5) to (7) together with eqns (1-3) have been used to calculate acceleration factors for the case of trapped moisture. Figure 10 shows the calculated acceleration factor relative to 85/85 test for decapsulated devices. From Figure 10 it is evident that the acceleration factor will decrease as the test temperature appoaches the Dew Point.

Assuming a median life of 24h for decapsulated devices in an 85/85 test, an acceleration factor of 4×10^4 is required if the field median life requirement is to be 10^6h. This in turn implies that devices with a moisture content of ≤ 2000 ppm_v could be used above -18^oC.

FIELD FAILURES OF NONHERMETIC MOS-MEMORIES DUE TO CORROSION

11628 units of 1k PMOS dynamic RAM's in CERDIP encapsulation were kept under surveillance by a failure reporting routine. The dominating failure mode was corrosion on a V_{DD}-line very close to a V_{SS}-line where the field strength was 2.7 V/um. All corroded devices were found to be nonhermetic.

Figure 11 shows the cumulative failures as a function of time. The median life of the nonhermetic parts is estimated to be 1.5×10^4 h for T = 30°C and RH = 50%. According to Figure 8 the acceleration factor for 30/50 is 2000.

The median life at 85/85 would then be $1.5 \times 10^4/2000 = 7.5$ h. This has so far not been tested but the estimate is in agreement with the 15 h median life of CMOS at 85/85 from Figure 4. Thus it is concluded that the median life of non hermetic MOS-memories can be estimated by using the acceleration factors of Figure 5 or 8.

CONCLUSIONS

1. It has been shown that plastic encapsulated semiconductors can not be approved for general use in telecommunication applications. They may, however, be used in cases where the chip temperature exceeds the room ambient by at least 10°C.

2. Acceleration factors for different combinations of temperature and humidity have been collected and two models are found useful for prediction purpose. It is proposed that THB tests should be evaluated using one of these two models and that the slopes of Figures 5 and 8 should be used.

3. Hermetic encapsulated devices should have $\leq$2000 ppm_v of trapped moisture within the cavity. (Dew Points $\leq$-20°C at 0.5 Atm cavity pressure).

4. Nonhermetic CERDIP-encapsulated MOS-memories have caused field failures within 2 years. The mediam life of non hermetic microcircuits can be estimated by using the acceleration factors of Figure 5 or 8 on results from decapsulated devices tested at 85/85.

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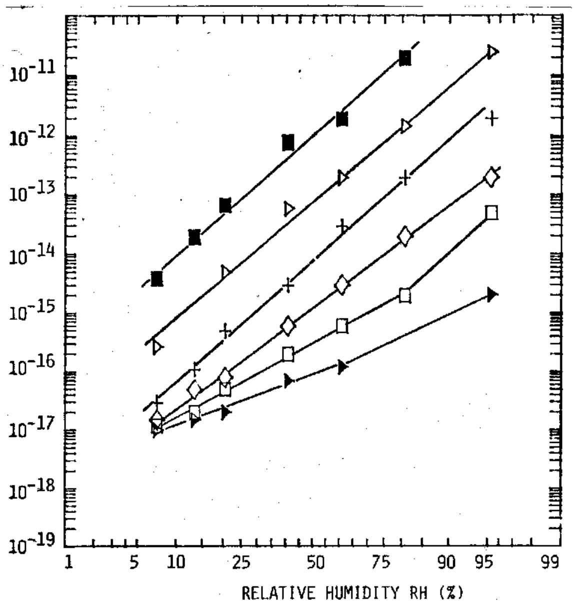

FIGURE 1

PLOT OF SURFACE CONDUCTIVITY AS A FUNCTION OF RELATIVE HUMIDITY AND TEMPERATURE ACCORDING TO REF 1 FIG 10A.

■ = 95°C
▷ = 80°C
+ = 65°C
◇ = 50°C
□ = 23°C
▶ = 10°C

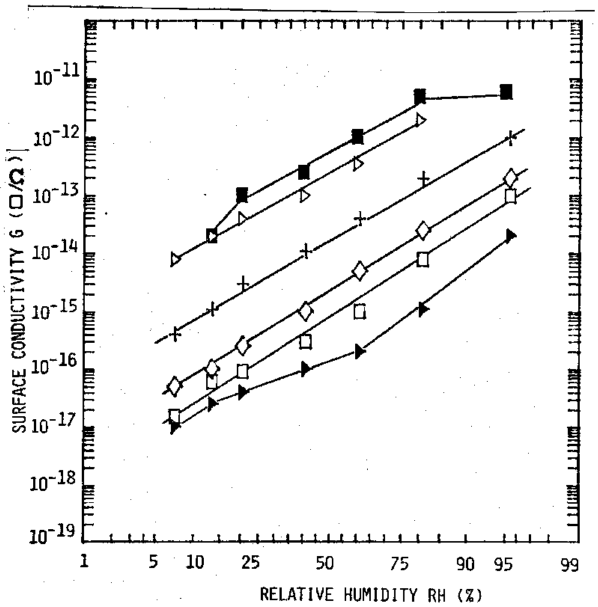

FIGURE 2

PLOT OF SURFACE CONDUCTIVITY AS A FUNCTION OF RELATIVE HUMIDITY AND TEMPERATURE ACCORDING TO REF 1 FIG 10B. ENCAPSULATED DEVICES.

□ = 95°C
▷ = 80°C
+ = 65°C
◇ = 50°C
□ = 23°C
▶ = 10°C

E2-4

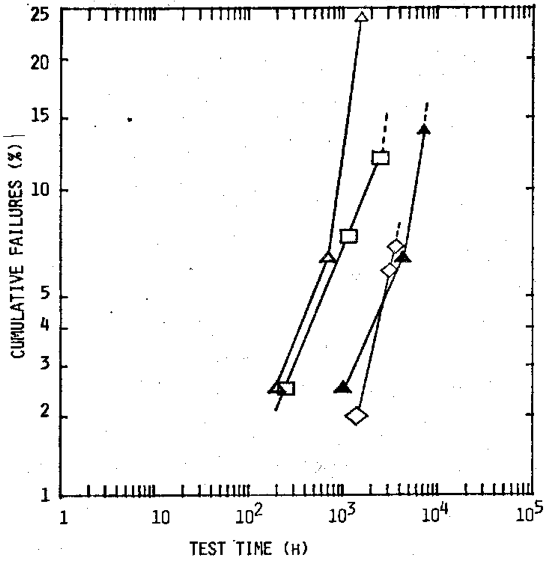

FIGURE 3

CUMULATIVE AMOUNT OF FAILURES (%) AS A FUNCTION OF TEST DURATION ON PLASTIC ENCAPSULATED CMOS DEVICES IN DIFFERENT ENVIRONMENTS.

△ : 85°C/85 % RH
□ : 65°C/95 % RH
◇ : 65°C/85 % RH
▲ : 45°C/95 % RH

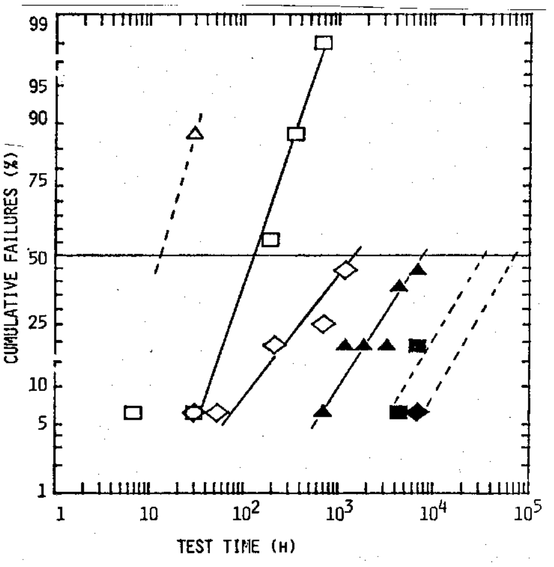

FIGURE 4

CUMULATIVE AMOUNT OF FAILURES (%) AS A FUNCTION OF TEST DURATION ON DECAPSULATED CMOS DEVICES IN DIFFERENT ENVIRONMENTS.

△: 85°C/85% RH
□: 85°C/55% RH
◇: 85°C/20% RH
▲ : 20°C/85% RH
■ : 20°C/58% RH
◆ : 20°C/26% RH

E2-10

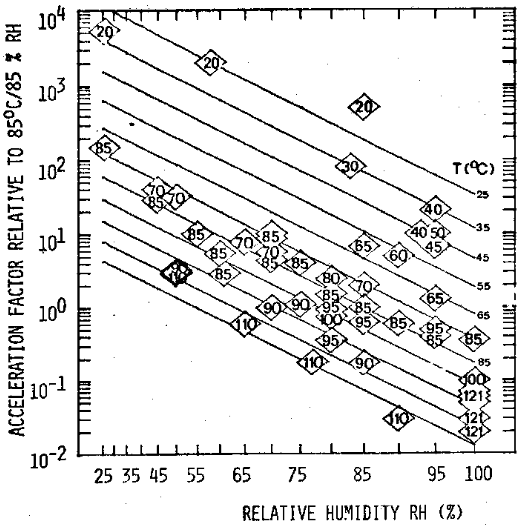

FIGURE 5

ACCELERATION FACTOR OF HUMIDITY TESTS RELATIVE TO MEDIAN LIFE AT 85°C/85 % RH.

◇T: RESULTS ACCORDING TO DIFFERENT TESTS (SEE TEXT)
——: CALCULATED USING THE $(RH)^2$ - MODEL WITH
$E_A = 0.8$ eV
SLOPE = LOG $60/(85^2-25^2)$

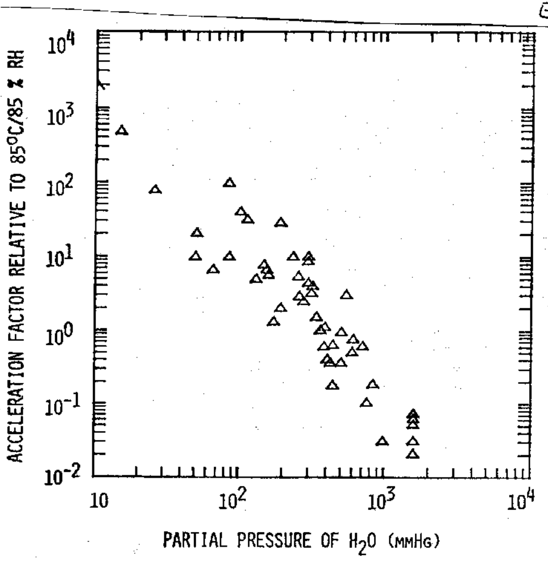

FIGURE 7

ACCELERATION FACTORS RELATIVE TO TESTS AT 85°C/85 % RH PLOTTED AS A FUNCTION OF LOG V_P. THE MODEL DOES NOT SEEM TO HAVE AN ADEQUATE ACCURACY.

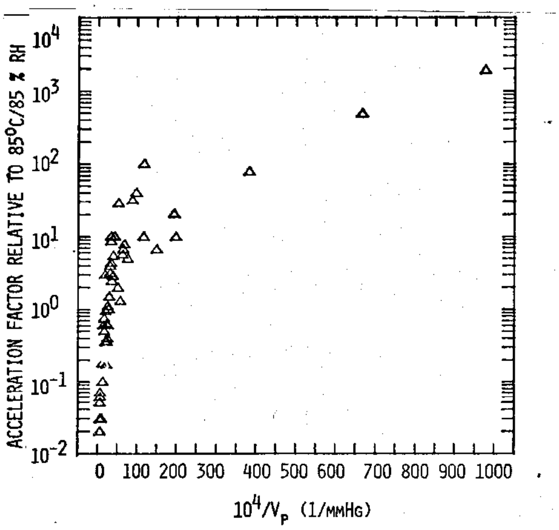

FIGURE 6

ACCELERATION FACTORS RELATIVE TO TESTS AT 85°C/85 % RH PLOTTED AS A FUNCTION OF THE INVERTED VALUE OF WATER VAPOR PARTIAL PRESSURE TIMES 10 000. THE MODEL DOES NOT SEEM TO BE USEFUL FOR PREDICTION PURPOSE.

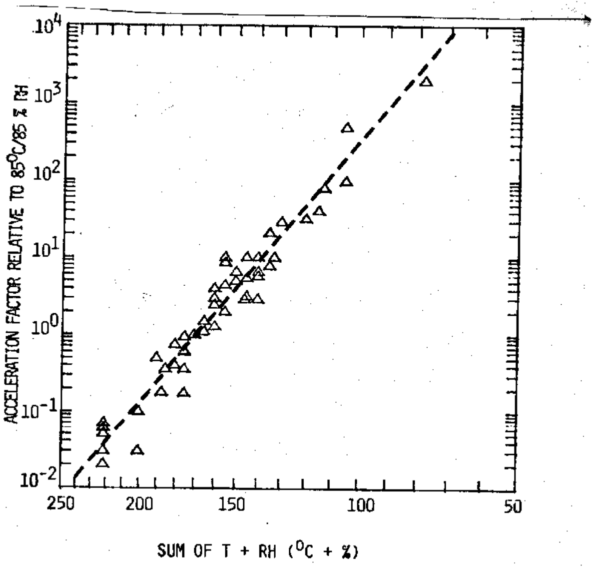

FIGURE 8

ACCELERATION FACTORS RELATIVE TO 85°C/85 % RH PLOTTED AS A FUNCTION OF THE NUMERICAL SUM OF T(°C) AND RH(%). IN AN ARRHENIUS DIAGRAM USING THAT SUM INSTEAD OF THE TEMPERATURE ALONE. THE MODEL IS PROPOSED BY REICH-HAKIM (REF 6) AND SEEMS TO BE USEFUL.
THE AVERAGE ACCELERATION FACTOR A FOLLOWS THE EQUATION

$$A = 2.9 \times 10^{-14} \exp(13810/(T(^{\circ}K) + RH(\%)))$$

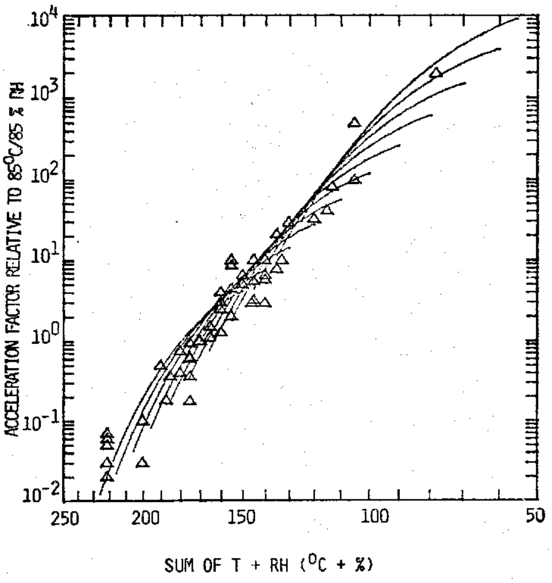

FIGURE 9

COMPARISON BETWEEN THE (T+RH)-MODEL AND THE $(RH)^2$-MODEL. THE SOLID LINES ARE CALCULATED ACCORDING TO EQUATIONS (1) - (3) AND THE FIGURE SHOWS THAT THE TWO MODELS ARE SUPPORTING EACH OTHER.

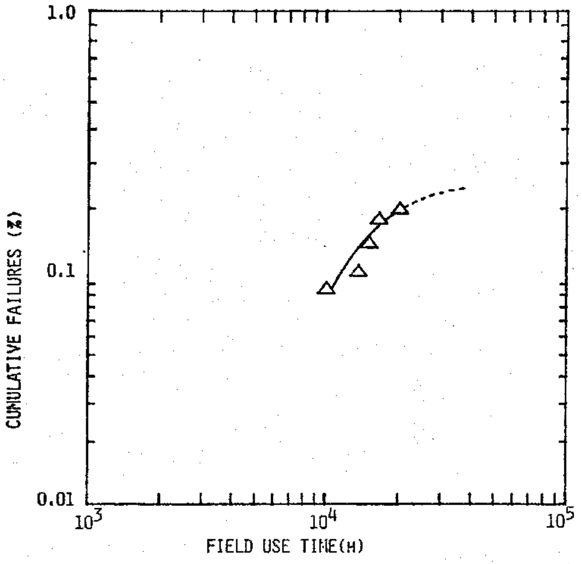

FIGURE 11

CUMULATIVE FAILURES DUE TO CORROSION OF UNHERMETIC PMOS 1K MOS-RAM's. THE TOTAL AMOUNT IS ESTIMATED TO 0.24 % AND MEDIAN LIFE (0.12 %) IS ESTIMATED TO $1.5 \cdot 10^4$(H). THE ENVIRONMENT AROUND THE MICROCIRCUIT WAS T = 30°C AND RH = 50 %.

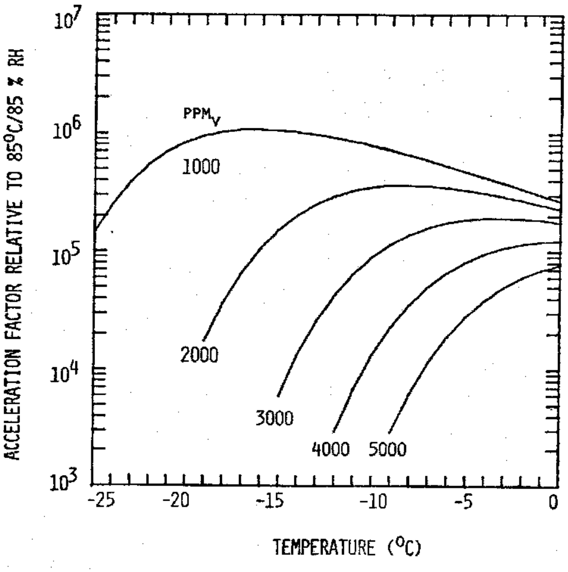

FIGURE 10

ACCELERATION FACTORS AS A FUNCTION OF TEMPERATURE FOR HERMETIC DEVICES WITH TRAPPED MOISTURE AT 380 MMHG CAVITY PRESSURE RELATIVE TO TESTS AT 85°C/85 % RH OF DECAPSULATED DEVICES.

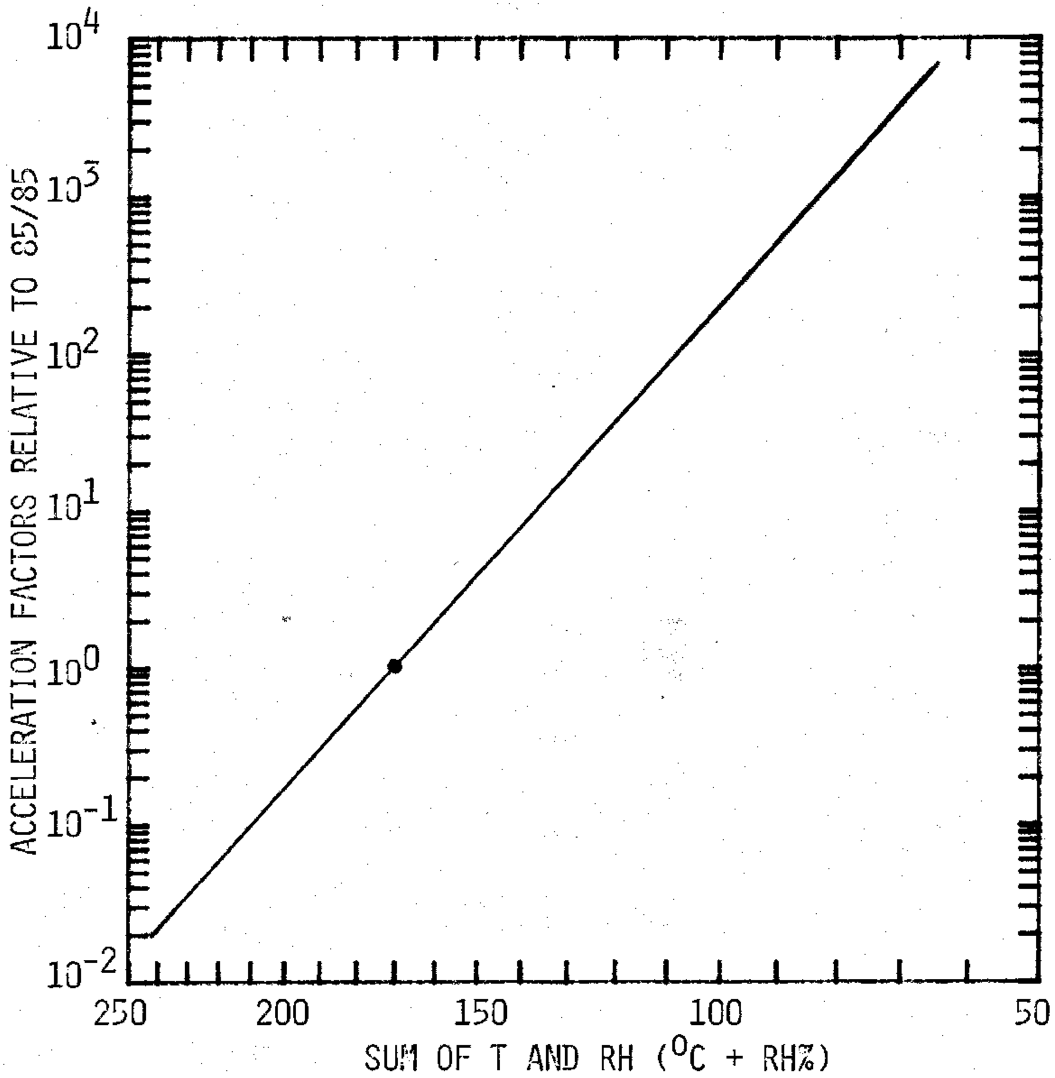

FIGURE 1

ACCELERATION FACTORS FOR THB-TESTS RELATIVE TO 85/85. THE LINE IS A CONSERVATIVE ESTIMATE OF THE AVERAGE VALUE FROM A NUMBER OF DIFFERENT THB-TESTS (REF. 2)